WHAT IS CLAIMED IS

~~Patent claims~~

1. Bus system produced by bundling several individual lines or buses or subbuses (see Figures 4, 5) within a unit of the DFP, FPGA or DPGA type as well as all units having a two- or multi-dimensional programmable cell architecture (see Figures 1, 2, 3) by means of which multiple units can be combined and/or memories and/or peripherals can be connected (see Figure 10).

2. Bus system according to Claim 1, characterized in that one or more interfaces (Figures 6, 7) assume the function of combining the lines and create the bus system.

3. Bus system according to Claims 1 and 2, characterized in that one or more state machines (0703/0603) control the interfaces (see Figures 6, 7).

4. Bus system according to Claims 1, 2 and 3, characterized in that the state machine also controls the external bus.

5. Bus system according to Claims 1 and 2, characterized in that there is an address generator (0610/0710) which generates the addresses for the units to be contacted via the bus.

6. Bus system according to Claims 1 and 2, characterized in that the interfaces use one or more internal bus systems which may comprise multiple lines (see Figures 4, 5) for reading and writing (see Figure 9a, I-BUS).

7. Bus system according to Claims 1 and 2, characterized in that the interfaces use one or more internal bus systems which may comprise multiple lines

(see Figures 4, 5) for either reading or writing (see Figure 9b, II-BUS, IO-BUS).

8. Bus system according to Claims 1 and 2, characterized in that the interfaces operate one or more internal bus systems which may comprise multiple lines (see Figures 4, 5) in hybrid operation according to claims 6 and 7.

9. Bus system according to Claims 1 and 2, characterized in that there is one register for managing and controlling the bus system (EB-REG 0702, 0602).

10. Bus system according to Claims 1 and 2, characterized in that the bus is controlled by a unit (E-BUS MASTER) which accesses a plurality of lower-level units (E-BUS SLAVE).

11. Bus system according to Claims 1, 2 and 10, characterized in that the bus control is transferred dynamically from one unit (E-BUS MASTER) to another (MASTER record in EB-REG).

12. Bus system according to Claims 1, 2, 10 and 11, characterized in that a lower-level unit (E-BUS SLAVE) can request the bus control (record of REQ-Master in EB-REG).

13. Bus system according to Claims 1 and 2, characterized in that there is a register indicating whether data are stored in the interfaces (SET-REG, 0612, 0712).

14. Bus system according to Claims 1 and 2, characterized in that the interfaces are either implemented directly on the unit or are created by the configuration of logic cells, i.e., cells in DFP, FPGA,

DPGA or similar units which fulfill simple logical or arithmetic functions according to their configuration.

15. Bus system according to Claims 1 and 2, characterized in that the interfaces can be configured by a primary logic unit and/or the unit itself (see Figures 8, 11).

16. Bus system according to Claims 1, 2 and 15, characterized in that the primary logic unit is partially integrated on the unit.

17. Bus system according to Claims 1 and 2, characterized in that standard bus systems can be used (see Figure 12).

18. Bus system according to Claims 1 and 2, characterized in that the unit has additional ordinary connections in the manner customary with DFPs, FPGAs, DPGAs, etc. (see Figure 12, 1201, 1204).

6.Definition of terms

ADR-GATE: Gate which switches addresses to the E-BUS if the unit is in E-BUS MASTER mode.

DFP: Data flow processor according to German Patent DE 44 16 881.

DPGA: Dynamically programmable gate array. Related art.

D flip-flop: Storage element which stores a signal at the rising edge of a clock pulse.

EB-REG: Register that stores the status signals between I-BUS and E-BUS.

E-BUS: External bus system outside a unit.

E-BUS MASTER: Unit that controls the E-BUS. Active.

E-BUS SLAVE: Unit controlled by the E-BUS MASTER. Passive.

E-GATE: Gate which is controlled by the internal state machine of the unit or by the E-BUS MASTER and switches data to the E-BUS.

E-GATE-REG: Register into which data transmitted to the E-BUS over the E-GATE is entered.

E-READ: Flag in the EB-REG indicating that the OUTPUT CELLS have been transferred completely to the E-BUS.

E-WRITE: Flag in the EB-REG indicating that the E-BUS has been transferred completely to the INPUT CELLS.

Flag: Status bit in a register, indicating a state.

FPGA: Field programmable gate array. Related art.

Handshake: Signal protocol where a signal A indicates a state and another signal B confirms that it has accepted signal A and responded to it.

INPUT CELL: Unit transmitting data from the E-BUS to an I-BUS.

I-BUSn *(also I-BUS)*: Internal bus system of a unit, which may also consist of bundles of individual lines, where n indicates the number of the bus.

II-BUSn *(also II-BUS)*: Internal bus system of a unit, which may also consist of bundles of individual lines, with n denoting the number of the bus. The bus is driven by an INPUT CELL and goes to logic inputs.

IO-BUSn *(also IO-BUS)*: Internal bus system of a unit, which may also consist of bundles of individual lines, with n denoting the number of the bus. The bus is driven by logic outputs and goes to an OUTPUT CELL. n indicates the number of the bus.

I-GATE: Gate that switches data to the I-BUS.

I-GATE-REG: Register which is controlled by the internal state machine or by E-BUS MASTER and into which data transmitted over the I-GATE to the I-BUS is entered.

I-READ: Flag in the EB-REG indicating that the INPUT CELLs have been completely transferred to the I-BUS.

I-WRITE: Flag in the EB-REG indicating that the I-BUS has been completely transferred to the OUTPUT CELLs.

Edge cell: Cell at the edge of a cell array, often with

direct contact with the terminals of a unit.

Configuring: Setting the function and interconnecting a logic unit, a (FPGA) cell (logic cell) or a PAE (see reconfiguring).

Primary logic unit (PLU): Unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed for this purpose.

Latch: Storage element which usually relays a signal transparently during the H level and stores it during the L level. Latches where the function of levels is exactly the opposite are sometimes used in PAEs. An inverter is then connected before the clock pulse of a conventional latch.

Logic cells: Configurable cells used in DFPs, FPGAs, DPGAs, fulfilling simple logical or arithmetic functions, depending on configuration.

MASTER: Flag in EB-REG showing that the E-BUS unit is a MASTER.

MODE PLUREG: Register in which the primary logic unit sets the configuration of an INPUT/OUTPUT CELL.

OUTPUT CELL: Unit that transmits data from an I-BUS to the E-BUS.

PAE: Processing array element: EALU with O-REG, R-REG, R20-MUX, F-PLUREG, M-PLUREG, BM UNIT, SM UNIT, sync UNIT, state-back UNIT and power UNIT.

PLU: Unit for configuring and reconfiguring a PAE or a logic cell. Embodied by a microcontroller specifically designed for this purpose.

REQ-MASTER: Flag in the EB-REG indicating that the unit would like to become E-BUS MASTER.

RS flip-flop: Reset/set flip-flop. Storage element which can be switched by two signals.

SET-REG: Register indicating that data has been written in an I-GATE-REG or E-GATE-REG but not yet read.

STATE-GATE: Gate switching the output of the SET-REG to the E-BUS.

Gate: Switch that relays or blocks a signal. Simple comparison: relay.

Reconfiguring: New configuration of any number of PAEs or logic cells while any remaining number of PAEs or logic cells continue their own function (see configuring).

State machine: Logic which can assume miscellaneous states. The transitions between states depend on various input parameters. These machines are used to control complex functions and belong to the related art.

7. Conventions

7.1.Naming conventions

Unit: -UNIT
Operating mode: -MODE
Multiplexer: -MUX
Negated signal: not-
Register for PLU visible: -PLUREG
Internal register: -REG
Shift registers: -sft

7.2Function convention

Shift registers: sft

AND function: &

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

OR function: #

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

NOT function: !

A	Q
0	1
1	0

GATE function: G

EN	D	Q
0	0	-
0	1	-

EN	D	Q
1	0	0
1	1	1

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